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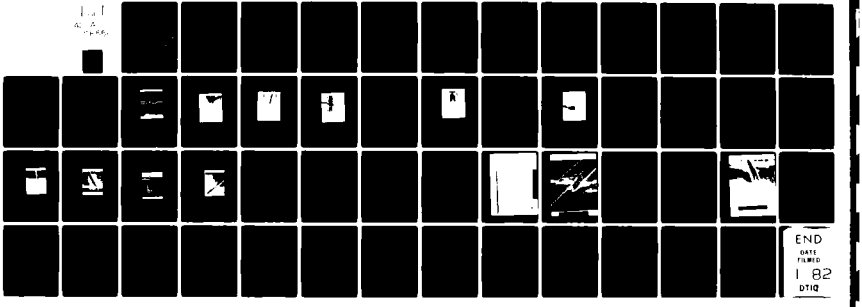

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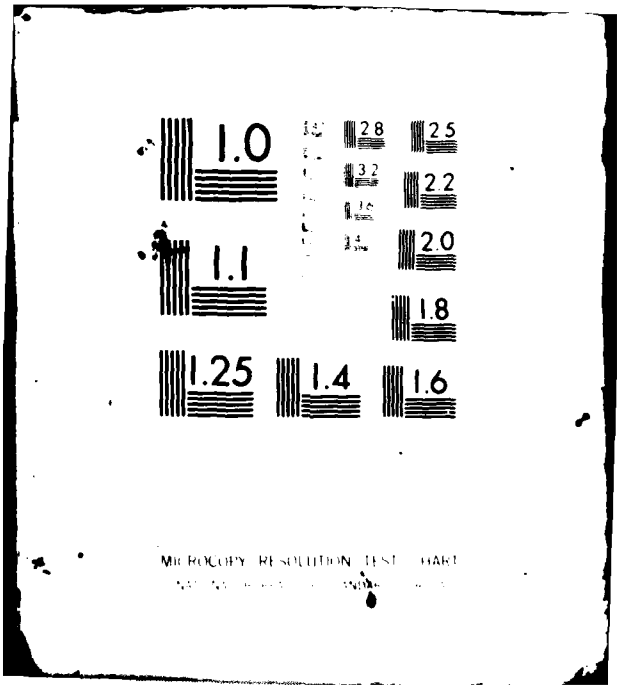
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SUBMICRON FETs USING MOLECULAR BEAM EPITAXY

FINAL REPORT

October 1981

Prepared by:

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CONTRACT N00014-77-C-0655

Contract Authority NR 251-027

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: Final Report	2. GOVT ACCESSION NO.: AD-A108556
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): Submicron FETs Using Molecular Beam Epitaxy	5. TYPE OF REPORT & PERIOD COVERED: Final Report August 1977--September 1981
	6. PERFORMING ORG. REPORT NUMBER:
7. AUTHOR(s): S. Bandy, Y. Chai, R. Chow, T. Gibbs, C. Hooper, C. Nishimoto and P. Stonestrom	8. CONTRACT OR GRANT NUMBER(s): N00014-77-C-0655
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Varian Associates, Inc. 611 Hansen Way Palo Alto, CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE 62762N RF 62-581-001 NR 251-027
11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Naval Research 800 N. Quincy Street Arlington, VA 22217	12. REPORT DATE: October 1981
	13. NUMBER OF PAGES: 50
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office): DCASMA - San Francisco 1250 Bayhill Drive San Bruno, CA 94066	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Low-noise GaAs FET, MBE GaAs, electron-beam exposure, gate resistance

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Electron-beam exposure and MBE material have been used to achieve quarter-micron gate length GaAs FETs. A noise figure of 1.1 dB with an associated gain of 14 dB has been measured at 8 GHz, the result of using a new mushroom gate profile for the gate.

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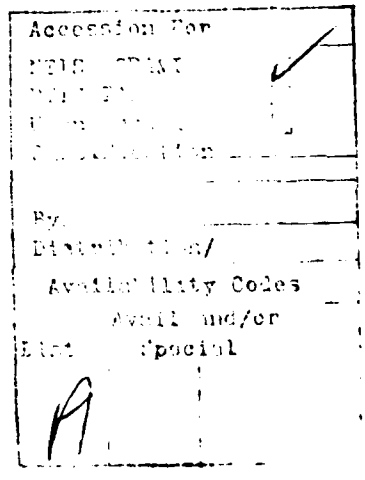
FOREWORD

The work reported here was supported by the Office of Naval Research, Washington, D.C., under contract N00014-77-C-0655, and managed by Mr. Max Yoder. The program was aimed at developing FETs with gate lengths of around 0.25 micron and looking for any evidences of velocity overshoot.

The work was carried out in the Varian Corporate Research Solid State Laboratory. The authors wish to thank M. Pustorino and S. Lombardi for technical assistance. Valuable discussions with M. Yoder, R. Bell and L. Lamont are gratefully acknowledged.



SUMMARY

Using electron-beam exposure and MBE GaAs, FETs have been fabricated with gate lengths of around 0.25 micron. A noise figure of 1.1 dB with an associated gain of 14 dB has been measured at 8 GHz. A new technique to increase the gate cross-sectional area by employing a mushroom gate profile reduced the gate resistance by about a factor of six, but this dramatic reduction in input resistance resulted in only 0.2-0.3 dB improvement in the measured minimum noise figure. Because of this, it is felt that there is a problem of matching such a high Q input with the rather lossy microstrip technique used, resulting in an inaccurate measurement of the noise figure.

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I. INTRODUCTION

A portion of the Introduction to Annual Report No. 2 will be repeated here, followed by a brief summary of the accomplishments up to the end of that reporting period and the problem areas to be dealt with as perceived at the start of this reporting period.

"Transient velocity overshoot" was proposed by Ruch[1] in 1972 to explain why GaAs, while having only a marginal advantage over Si with regard to the saturated drift velocity in the high field region (Fig. 1), is able to outperform Si in a FET structure. Cold electrons injected at the source may never reach their steady-state velocity before being collected at the drain, but travel at a higher velocity, approximately

$$v = \mu_0 E \qquad (1)$$

where μ_0 is the low field mobility, before relaxation effects take place. This transient phenomenon is due to the disparity between the energy and momentum relaxation times, causing the average velocity in the channel to overshoot its usual saturation value.

Figure 2 shows a computed plot of velocity vs. distance down the channel for both GaAs and InP, assuming a constant field.[2] These plots illustrate the significant role that velocity overshoot can play in increasing the effective electron velocity in submicron gate devices. Silicon also shows velocity overshoot, but the improvement is much smaller and would require gate lengths less than 1000 Å to realize it.[1] It may thus be possible to increase the effective saturated velocity in the FET channel without resorting to "super velocity" materials, by reducing the gate length of GaAs FETs.

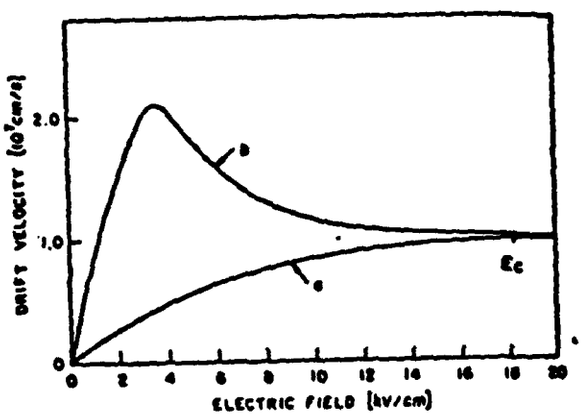


Fig. 1 Velocity-field characteristics in GaAs and silicon.[1)]

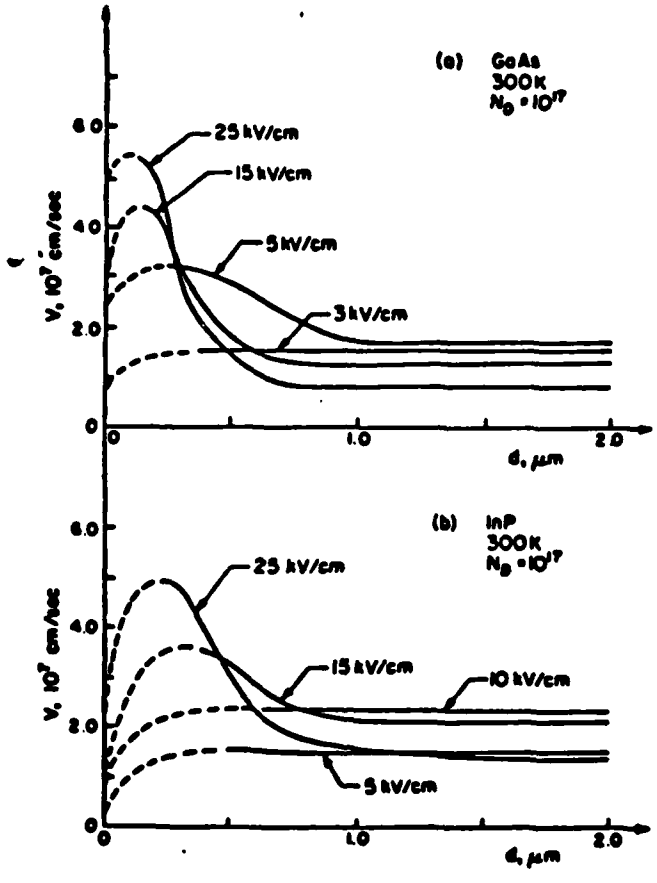


Fig. 2 Instantaneous velocity vs distance for 300°K, $N_a = 10^{17}$; (a) GaAs, (b) InP.[2]

It may well be that the proposed performance advantages of "super velocity" alloys such as InGaAsP will only be realized by the mechanism of velocity overshoot. As shown by the computations of Littlejohn, et al.[3] in Fig. 3, while the computed static velocity-field characteristic of InGaAsP shows a higher low field mobility, which can be utilized by velocity overshoot according to Eq. (1), the velocity in the high field region is less than that of GaAs. Thus, the investigation of the transient effects of velocity overshoot for other materials such as InP, InGaAs, InGaAsP and other promising materials is also a matter of importance.

In addition to the benefits available from higher carrier velocities in the channel, FET performance is, of course, improved directly by scaling down dimensions. However, besider the ability to provide quarter-micron openings in resist with electron beam photolithography, the gate metallization scheme must preserve the resist profile, the active layer must be thinner to prevent g_m reduction (Annual Report No. 1 of this contract), and the effective source-gate spacing must be reduced to avoid source resistance domination. In addition to all this, it may be that a reduction in device width or the addition of multiple gate pads may be necessary to overcome the increased gate resistance brought about by using such small gate lengths. If a narrower-width device is used, it may be necessary to integrate a driver FET of larger dimensions on the same chip to drive the off-the-chip parasitics involved in the realization of practical broadband microwave amplifiers (being a second stage, its gain and noise figure are of less importance).

Concerning the progress in rf performance at the start of this reporting period, a minimum noise figure of 1.2 dB with an associated gain of 13 dB had been achieved. These results were the best obtained for MBE material as reported in the literature to date, and were primarily accomplished by going from one to two gate pads. The parameter limiting device performance was still primarily the gate resistance,

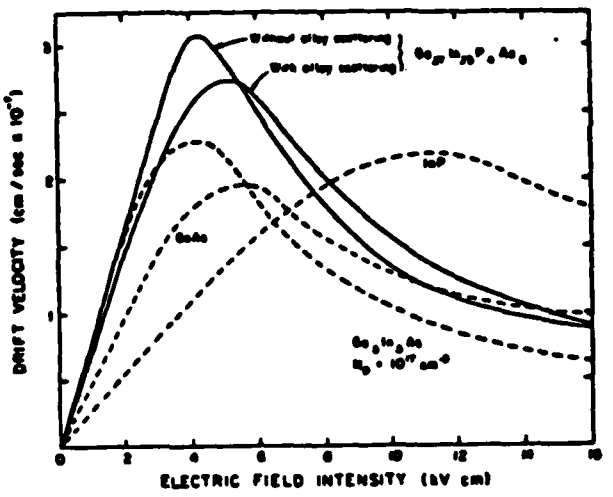


Fig. 3 Velocity-field characteristic of $Ga_{0.27}In_{0.73}P_{0.4}As_{0.6}$ with and without random potential alloy scattering. Shown for comparison are the velocity-field curves for GaAs, InP, and $Ga_{0.5}In_{0.5}As$. The doping level is $10^{17} cm^{-3}$. 3)

which was high because of the small gate metal cross section, caused in turn by the resist opening being gradually closed by metal buildup on the resist edge during the evaporation.

The first task to be addressed on the current phase of the contract was to continue work on developing the mushroom-type gate profile, thereby increasing the gate cross-sectional area and reducing the gate resistance, r_g. Thus far there have been yield problems, primarily due to performing a sequence of operations without being able to monitor them visually. Other items in need of consideration are reducing the source resistance, R_s, and source inductance, L_s, investigation of possible electron-beam damage in the gate region, and elimination (or at least investigation) of the observed phenomenon of transconductance reduction in going from dc to the GHz range.

Once r_g and R_s have been sufficiently reduced to allow study of the properties of the intrinsic device, the ultimate goals of this contract can be addressed:

(1) determination of the optimum channel thickness and doping for a given gate length,

(2) fabrication on different crystalline orientations to observe any anisotrophy of the electron velocity overshoot effect that may occur; this will be done by determining the effective saturation drift velocity, v_s, by the techniques developed under ONR Contract N00014-77-C-0125[4] and described in the final report of that contract.

(3) evaluation of the use of an MBE AlGaAs buffer layer for carrier confinement to the active layer.

2. DEVELOPMENT OF MUSHROOM GATE TECHNOLOGY

The difficulty was mentioned in Annual Report No. 3 of obtaining reproducible results with the mushroom profile process for the gate which uses two layers of PMMA resist separated by a thin layer of Al. During the most recent period, a closer look was taken at the resist exposure and the metallization profiles.

2.1 Focusing Problems

A series of gate patterns were exposed, some with the electron beam refocused every fifth device and others with the focus being done on each device (which destroys the middle of the device, but at least the gate regions away from the focused area can be evaluated). It was found that the focus could change (although not usually) quite significantly between adjacent devices, which meant that the only way to guarantee good focus was to focus on every device. When every device was focused, the resist openings appeared to be the same, but since focusing destroys the device, it is not an acceptable solution.

The problem of the sensitivity of the double resist mushroom scheme to the focus was demonstrated by another run which was made where between each focus the line width remained constant, but changed after each focus. This demonstrated the degree of subjectivity in manual focusing.

An automatic focusing program was developed in this laboratory which enabled the LSI-II computer to focus the SEM. This will remove the subjective nature of discerning when good focus is achieved and render the process operator independent. The problem with the double resist scheme for the program, and probably also for doing the focus manually, is that the metal between the two resist layers smoothes out the surface features so that there are no sharp edges to focus on.

Nevertheless, it was felt that the automatic focusing program enabled a higher yield to be obtained for actual device runs than if the focusing had been done manually. However, the yield was still low.

It was also noted that the beam current would change gradually as devices were exposed, so pains were taken to keep it constant at 0.2 ± 0.01 nA. If allowed to deviate 0.03 nA, a change in the exposed resist could be detected optically.

Subjectively, it appears that the double resist scheme is much more sensitive to drift in both the focus and the condenser current than is the conventional single-resist layer approach.

2.2 Void Formation

Observation of the metallized gate patterns (Al) after resist lift-off also reveals the interesting phenomenon shown in Fig. 4. The micrograph of Fig. 5 illustrates Fig. 4(a), Fig. 6 illustrates Fig. 4(c), and Fig. 7 is a result of Fig. 4(d). To be noted is the transition from Fig. 4(a) to Fig. 4(c) in Fig. 8, as the gate crosses the mesa edge (this can also be seen in Fig. 5). The change in slope of the top of the mushroom as it crosses the mesa in Fig. 5 is interesting. Perhaps because of the thicker resist (assuming the top of the resist is level as it crosses the mesa edge), the vapor pressure of residual water is higher in the resist opening off the mesa (discussed in connection with g_m compression in Annual Report No. 3), which in turn reduces the lateral diffusion mobility of evaporated atoms.

Figures 4-8 appear to indicate that the best mushroom profiles are obtained when there is no channel etch. The profile degenerates as the channel etch increases until it becomes simply a triangle with the deepest channel etch. Although it is true that this study was done on

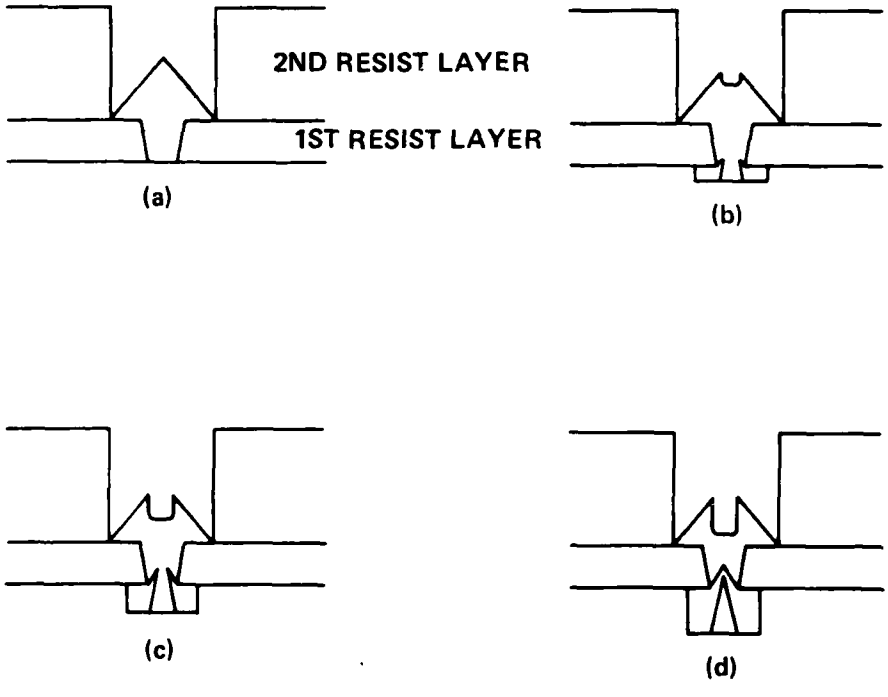


Fig. 4 Effect of channel etch on mushroom gate profile.

Fig. 5 Illustration of Fig. 4(a).

Fig. 6 Illustration of Fig. 4(c).

Fig. 7 Illustration of Fig. 4(d).

Fig. 8 Transition from Fig. 4(a) to Fig. 4(c) as the gate crosses the mesa edge.

a dummy wafer and the channel etch may have been a little deep, it seems clear that the problem of closure of the resist opening also plagues the mushroom gate process. Figure 9 reveals that even with no channel etch, a triangle shape can be seen imbedded in the mushroom cross-section. This is probably due to the gap between the bottom of the resist and the top of the GaAs due to the 1000 Å thick SiO_2 layer (not shown in Fig. 4), with Fig. 10 illustrating how this gap propagates a void in the deposition. This discontinuity evidently is not a true void, since the top of the mushroom appears solidly attached to its base, but becomes a true void as the channel is etched. Figure 11 shows a case where in the act of cleaving the wafer, the top portion of the gate was separated from its base. Whereas the mushroom structure was proposed in order to circumvent the problem of closure of the resist opening by the metallization, it now appears that this problem is going to have to be dealt with directly anyway to be able to form mushroom profiles in a recessed channel.

The problem of the channel not etching in places was felt to have been due to bad focus. If so, then the good mushroom gate profiles obtained so far have been badly focused gates. When the focus is good, the channel etches, and the resulting gate profiles are either triangular or similar to Fig. 6.

2.3 Efforts to Reduce Lateral Surface Mobility

In the previous section, a case was made for having to deal with the problem of closure of the resist opening by the deposited metallization in spite of using the double-layer resist scheme to achieve a mushroom profile for the gate. In Annual Report No. 3, this problem was stated to be caused by the evaporated metal acting as a two-dimensional fluid flowing sideways out over the edge of the resist. Concerning this phenomenon, p. 178 of Chopra[5] states that Al has a lower adatom surface

Fig. 9 Mushroom cross-section showing faint triangle imbedded in base stem.

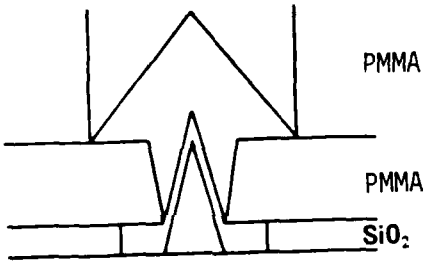


Fig. 10 Void propagation during deposition.

Fig. 11 Photo showing separation of the mushroom top from its base when cleaved.

mobility than Au, and indeed the problem of triangular gates was much less for Al than for Au, thus giving support for the belief that metal flow was the source of the problem. That report also described how a ceramic mask having a 1/4-inch opening was placed over the 1-cm diameter source boat, but in spite of the better collimation and the lower thermal radiation reaching the wafer, the problem of triangular gates remained virtually the same. This result was taken to mean that the energy of the evaporant atoms rather than thermal input from the source radiation was responsible for the lateral surface mobility of the atoms.

In the most recent reporting period, the first experiment tried was to evaporate Al both at 30 Å/sec and 3 Å/sec and compare the results. Although it is true that the lower rate will do little to change the atom's energy as it leaves the source, the background pressure will become more influential in reducing the kinetic energy of the atoms by the time they reach the wafer. Nonetheless, no difference was seen between the two rates with regards to steepening the sides of the triangular gates. Although the rate could be lowered further, it would result in an inordinately long evaporation. A better technique might be to do the evaporation at an elevated background pressure.

Even if the kinetic energy of the atoms was reduced to zero before impinging upon the wafer, the heat of condensation might be responsible for the lateral surface mobility, since the energy involved (1 to 4 eV for metals) is much higher than kT.[6,7] So the thinking was that perhaps rather than try to reduce the kinetic energy of the evaporant atoms to some minimal level, an effort should be made to dissipate the condensation energy by cooling the wafer. An evaporation run was done with the wafer cooled by clamping it to a metal block which had liquid nitrogen passing through it. A slight jar to the wafer after the evaporation caused all the Al to pop off in one sheet, indicating severe strain due to thermal mismatch when the wafer was warmed back to room temperature,

and also preventing any determination of whether or not the surface mobility had been significantly reduced.

Because both Au and Al have s-type outer shell configurations which are spherically symmetric, perhaps they tend to "roll" on the surface easier than would atoms having highly asymmetrical outer shell configurations. Pt has a d-type outer shell configuration which has very directionally localized bond angles, so its lateral surface mobility may be greatly reduced. If so, the base of the mushroom could be Pt with Au forming the wider top portion. A 2600 Å thick evaporation of Pt was tried with a single layer of resist, but evidently the heat generated widened the resist opening as the evaporation progressed, making it difficult to ascertain anything about the surface mobility. Perhaps reduction of the 10 Å/sec rate used would help alleviate this problem.

As a long shot, ~5000 Å of Al was sputtered in 30 sec to see if the very fast rate might impede the lateral mobility by immediately covering the atoms with additional evaporant. What in fact happened was the opposite -- the resist opening was closed off so rapidly by the metallization that almost no Al was deposited in the gate opening.

2.4 Source Collimation Using Baffles

In discussing with Larry Lamont of the Varian Vacuum Division what possible things might be tried next, he suggested that the problem might be geometrical after all. He recalled in Airco Temescal's book[8] a brief mention that for electron beam evaporation that a virtual source much larger than the actual source can exist as a result of collisions near the source. Supposing that this might also be true for boat evaporation, a series of 4 baffles were rigged as shown schematically in Fig. 12. Each baffle had a 3/8" hole in it, with all the holes in alignment directly above the source boat. The initial experiment used a thickness monitor directly above the top baffle to calibrate the deposition rate,

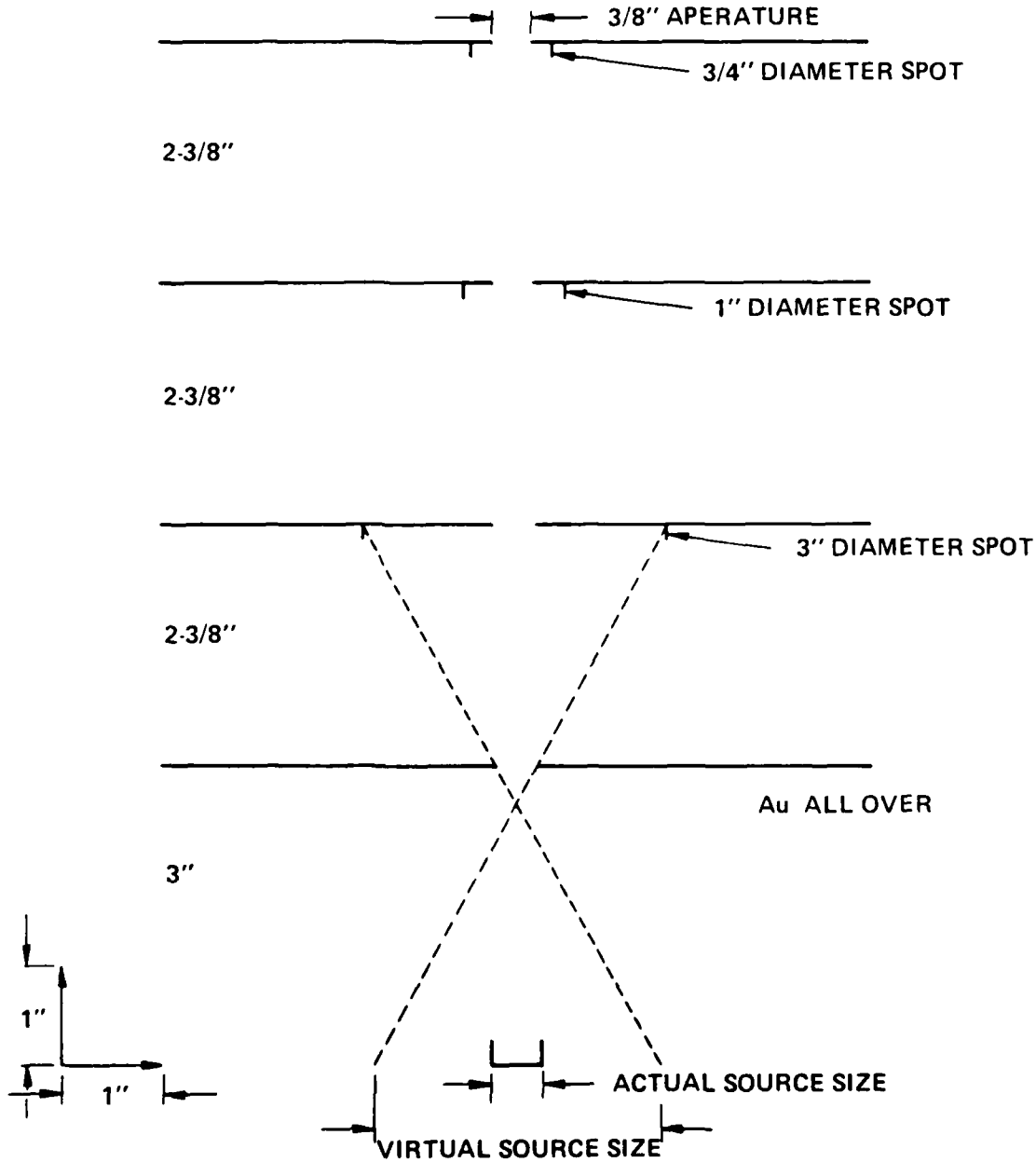
and the intention was to observe the bottom of each baffle plate to determine the extent of the evaporation in order to establish quantitatively if indeed a virtual source exists whose size was considerably larger than the actual source size.

Boat evaporation of Au at the rate of about 50 Å/min yielded the results shown in Fig. 12. The bottom baffle, as would be expected, was completely covered with Au on its bottom side. However, it was also observed that the next baffle plate had a 3" diameter Au spot on its bottom side rather than the ~1" diameter spot one would expect if all the Au came in a straight line from the 1/2" source. As shown in Fig. 12, this extrapolates back to a virtual source size of about 3" on the plane of the actual source. The remaining two baffles have spot sizes consistent with geometrical shadowing, indicating that there are no virtual sources formed above any of the baffle plates. The ~50 Å/min rate is about one-third of what the rate would have been without the baffles, indicating the significant contribution that the virtual source makes to the evaporation.

Figures 13, 14, and 15 show the results of a dummy Au evaporation run using the baffles with a single layer of PMMA. Figure 13 is before the gate liftoff, while Fig. 14 shows the gate after liftoff. Note the nearly rectangular profile which contrasts with the triangular profile obtained without the baffles. The gate in Fig. 13 is 0.25 micron long and 0.3 micron high. Without the baffles, 0.3 micron was about the height of the triangular cross-section obtained with Au for the same gate length. Al would give about 0.6 micron for the triangle height for the same gate length. In some places on the same wafer, triangular gates were in fact observed, although they had steeper sides than those obtained without the baffles (Fig. 15).

Figure 16 shows the result for the mushroom gate resist structure using the baffles with an Au evaporation. It can be clearly seen that the metallization sides are much steeper than without the baffles when compared with the unbaffled photos.

Fig. 12 Baffle arrangement demonstrating the presence of a virtual source during evaporation.



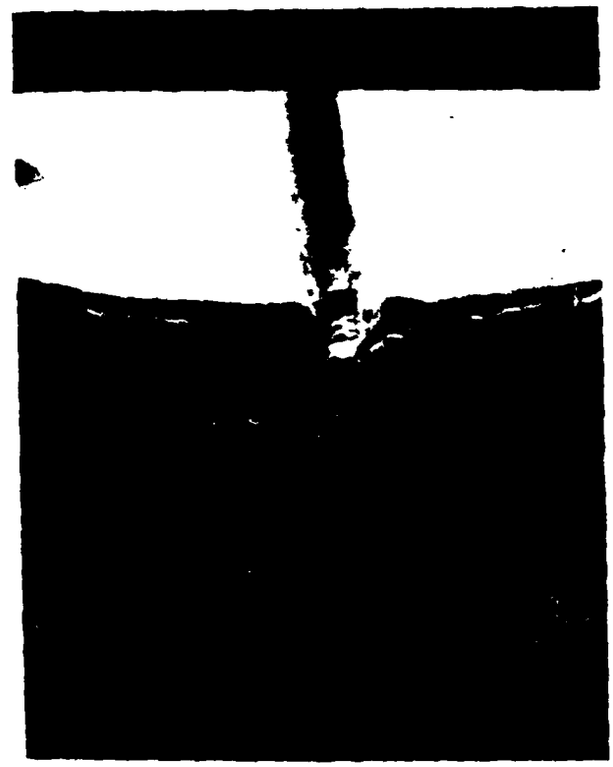


Fig. 13 Gate metallization profile using baffles before liftoff (2×10^4 magnification).

Fig. 14 Gate metallization using baffles (1.62×10^4 magnification).

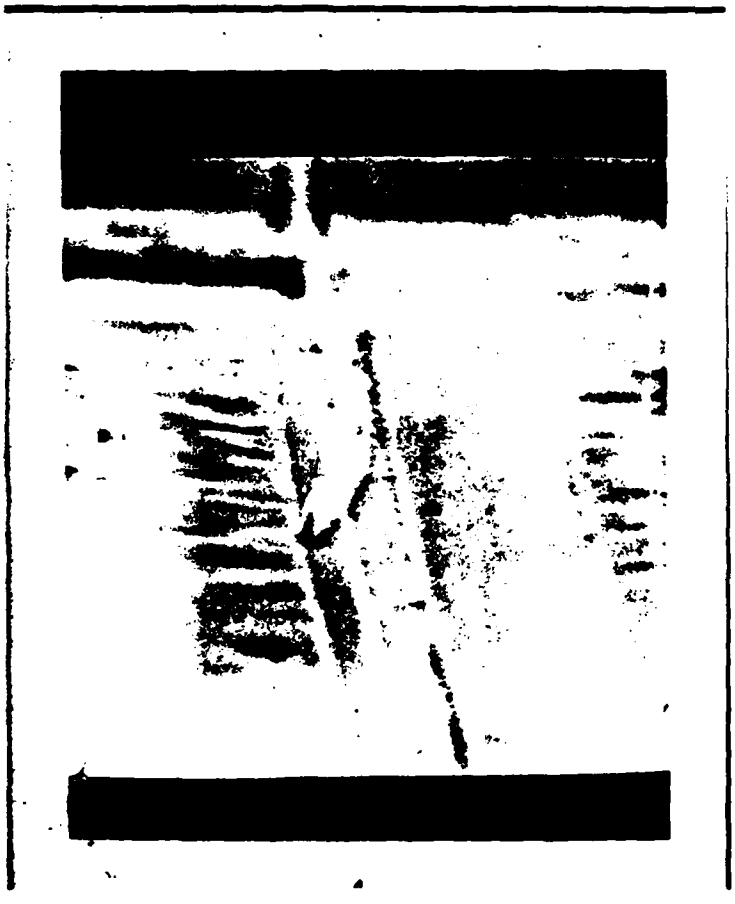


Fig. 15 Triangular gate appearance on same wafer as Fig. 3 (1.62×10^4 magnification).

Fig. 16 Mushroom gate using baffles (1.7×10^4 magnification).

To summarize, the use of baffles has demonstrated that a large virtual source exists, and that significantly steeper sides can be obtained for the gate metallization when the effects of this virtual source are eliminated. This is not to say that lateral surface mobility may still play a part in the problem, but it appears to be a much less significant effect.

3. g_m COMPRESSION REVISITED

In Annual Report No. 3 of this contract, we described the problems encountered with g_m compression when switching from Au to Ti/Pt/Au for the gate metallization. The conclusion reached then was that Ti and Al getter O_2 from the water vapor to form an oxide which then causes the g_m compression through interactions with interface states. The problem of water vapor was considered to be a problem for the E-beam FETs because of the very small gate opening. For a 0.2-μm aperture in the resist, the water contamination rate was computed to be 4300 Å/min, while for a one-micron aperture, it was only 170 Å/min.

During this period, the problem of g_m compression appeared even with the use of Au as the gate metallization. Until this time, g_m compression had never occurred with the use of Au except once or twice when the channel etch was greater than usual (e.g., run EB 25). Certainly Au cannot be considered to getter O_2, so the previous explanation cannot be considered to be adequate. In all cases, the forward characteristic of the gate revealed an insulating interface layer, as evidenced by a high turn-on voltage which could be broken down to give a normal forward characteristic. It was not clear why this problem surfaced with Au gates.

O_2 and CF_4 plasma treatments at various points in the process, as well as immediately before the gate metallization, did not help. It is hard to imagine an interface material existing after the citric acid channel etch; nevertheless, g_m compression existed when the Au gate metallization was put down immediately after the citric acid etch and DI rinse. The notion arose that perhaps the citric acid etch (which contains H_2O_2) when etching deeper becomes H_2O_2 dominant as the citric acid component becomes depleted (or the etch residue reduces its effective-ness), so that a net oxide is left when the etching is stopped. A

device run was tried with a dip in the citric acid etch containing no H_2O_2 after the regular citric acid etch, but g_m compression still persisted. It seems possible that citric acid won't etch oxide unless catalyzed by the H_2O_2.

Another possibility was that the initial deposition rate was slower, allowing more of the residual water vapor to be incorporated, which then reacts with the GaAs when the temperature rises as a result of the deposition. A faster initial deposition rate was implemented, and although subsequent runs have shown g_m compression, they have been on questionable wafers or have had bad ohmic contacts. However, several runs without g_m compression were made, so that it appears the evaporation rate is important. At any rate, run EB 29 was made (see next section) and it showed no g_m compression.

4. DEVICE RUN EB 29

Run EB 29 (MBE wafer #591) was the first run successfully employing the mushroom rate process using the two-level resist scheme. Figure 17 reveals no g_m compression. Figure 18 shows a typical gate for this run. Table I gives the rf data obtained for run EB 29, while Table II gives the rf data obtained for run EB 26 for purposes of comparison. Run EB 26 is the previous best run. Inspection of the tables indicates that on the average, the improvement in the measured minimum noise figure is around 0.2-0.3 dB.

To determine the gate resistance, the resistance was measured between the two gate pads, then doubled to obtain the total stripe resistance (which assumes the resistance of the leads to the pads is negligible) and then divided by 48 to give the effective FET gate series resistance. Table III shows the data obtained for random unbonded devices selected from both run EB 29 and run EB 26.

TABLE I

8-GHz Performance of Run EB 29

Device	NF_m (dB)	G_a (dB)
29-1	1.29	12
29-2	1.11	12.5
29-3	1.11	13.9
29-3 (different IF amplifier)	1.06	12.5
29-4	1.42 (10 GHz)	10.7 (10 GHz)

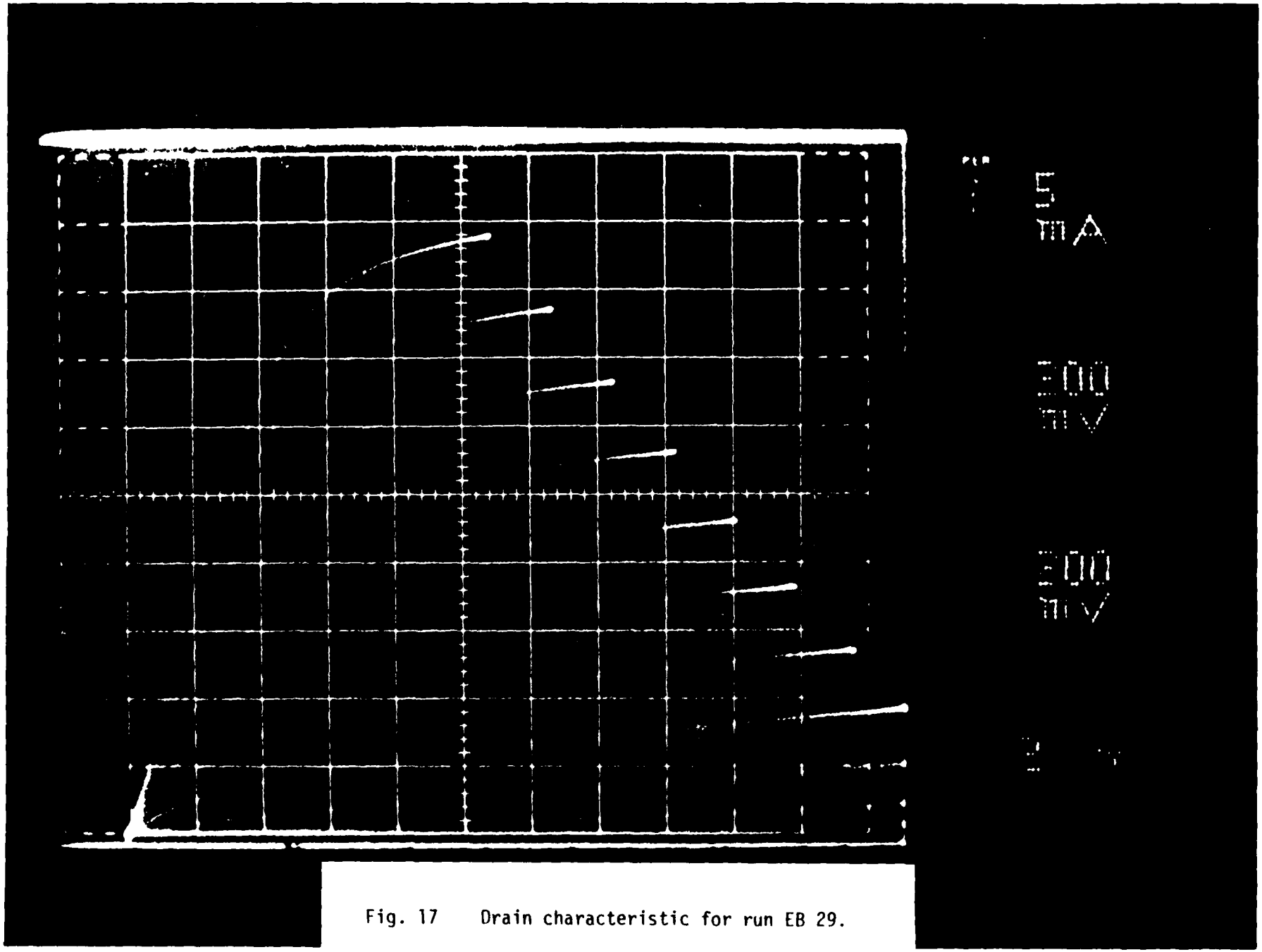


Fig. 17 Drain characteristic for run EB 29.

Fig. 18 Mushroom gate structure for run EB 29.

TABLE II

8-GHz Performance of Run EB 26

Device	NF_m (dB)	G_a (dB)
26-1	1.45	13.5
26-2	1.54	14.0
26-3	1.45	12.6
26-4	1.19	13.1
36-5	1.19	13.2

TABLE III

Gate Resistance for Runs EB 29 and EB 26

r_g for EB 29 (ohms)	r_g for EB 26 (ohms)
0.83	2.8
0.87	4.7
0.87	2.6
0.87	2.2
0.99	5.5
	5.5
	5.8

Table III clearly shows the improvement obtained in r_g using the mushroom gate structure. The lower values of r_g for run EB 26 correspond to gate lengths of 0.3-0.4 micron, so the higher values must correspond to the shorter gate lengths of the devices actually tested (0.19 micron for 26-3 and 0.16 micron for 26-4). The gate lengths for run EB 29 have not been measured because of the difficulty of doing so

in the presence of the mushroom top. It was even difficult to measure the gate length for the regular gate devices, since observation in the SEM invariably degraded the device characteristics. To measure the gate length for the mushroom structure necessitates cleaving the FET. Even so, when several of the FETs for which the measurements of Table II had been made were cleaved, the debris caused by the cleaving made it virtually impossible to determine gate lengths. An example is shown in Fig. 19. Is the gate length 0.18 micron or 0.32 micron? At any rate, for the devices rf tested, Table III shows about a factor of 6 improvement in gate resistance brought about by use of the mushroom gate process.

Table IV compares the source resistance R_s for runs EB 29 and EB 26, showing about a factor of two improvement. Also measured was the source-to-drain resistance measured on structures having no gate exposure for run EB 29 (i.e., no gate or gate recess, so that the n^+ layer extends uninterrupted from source to drain). This value was around 2.45 ohms, indicating at most half of that value (1.2 ohms) as the contribution to the source resistance of the n^+ layer and the ohmic contact. Since the gate recess is a significant fraction of the source-drain spacing (0.7 micron compared to 2.6 micron) and is usually offset towards the source, the contribution of the n^+ layer and contact resistance on the source side should be much less than half -- at most about one ohm. This leaves the gate-to-n^+ spacing as the dominant contributor to R_s, being about 2.5 ohms. Although it may be that the n^+ doping is higher for run EB 29 than for EB 26, the lower values of R_s for EB 29 are probably mainly due to the higher pinchoff voltage for run EB 29 (1.75 V vs 0.6 V) since it appears that the gate-to-n^+ spacing (about 1500 Å by Fig. 3) is the main contributor to R_s.

Based upon the dc values in Tables III and IV, $r_g + R_s$ is 4.4 ohms for EB 29 and 11.5 ohms for EB 26. This represents an improvement factor of 2.61, and assuming[9]

$$NF_m - 1 \propto (r_{in})^{1/2} \quad , \qquad (2)$$

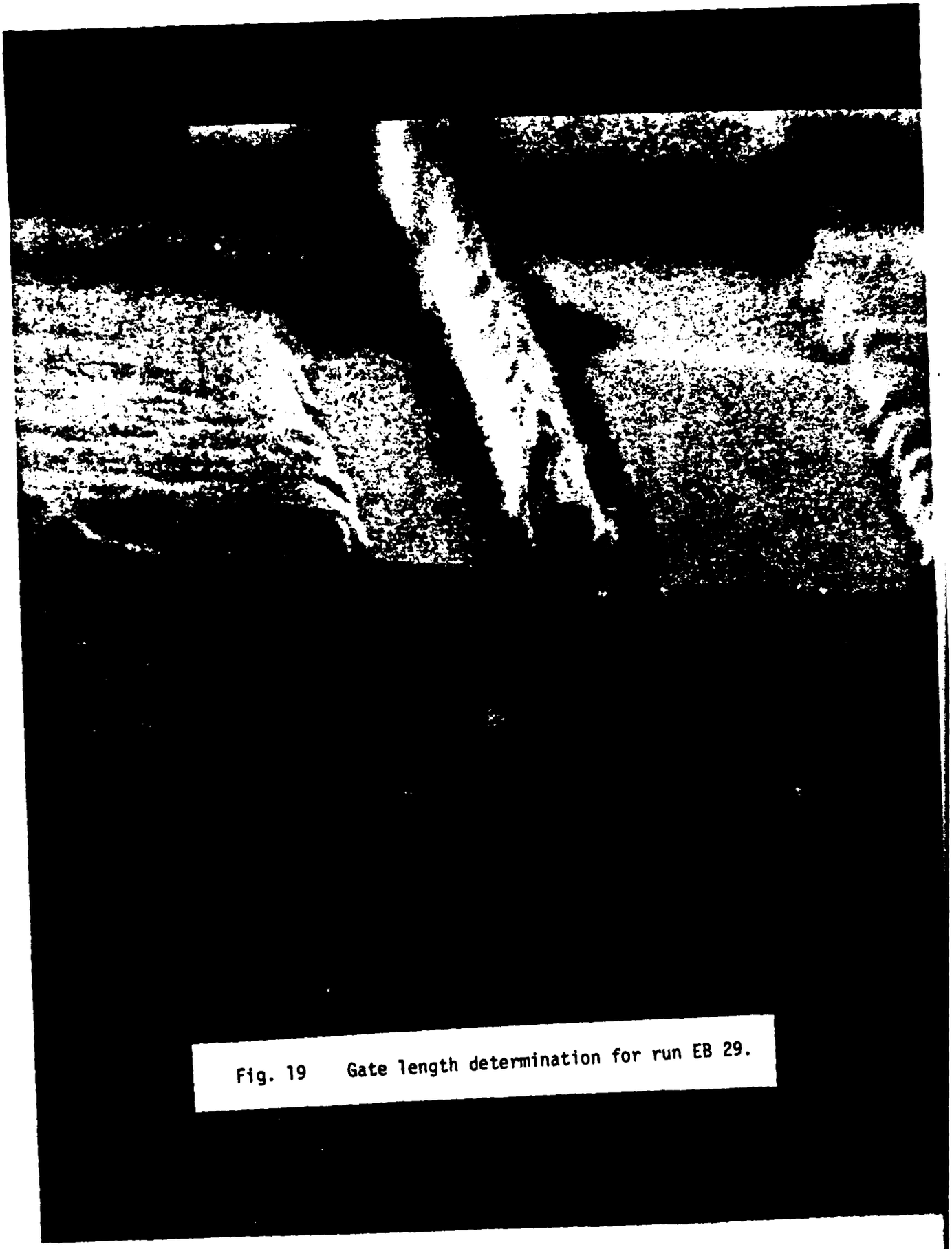


Fig. 19 Gate length determination for run EB 29.

TABLE IV

Source Resistance Comparison

Device	R_s (ohms)
26-1	6.35
26-2	6.15
26-5	5.2
29-1	3.5
29-3	3.4

then the 1.19-dB value for EB 26 should improve to 0.78 dB for EB 29. Perhaps the gate lengths are longer for EB 29. The devices of run EB 29 need to have their y-parameters measured and their drain characteristics need to be more fully analyzed.

For the low-noise measurements at 8 GHz, the input is matched by adjusting a capacitance which is a quarter of a wavelength away from the input along a microstrip line. According to Alan Podell, a Varian consultant, this is a very lossy technique to simulate inductance, and it seems probable that with the high Q input of the FETs (the mushroom gate of run EB 29 allowed an improvement in the input resistance of around a factor of 2.6), the low Q of the matching network does not permit an optimum noise match to be achieved at 8 GHz. Since the input Q will go down as the frequency is increased, a 26-GHz noise test setup is now being designed and assembled. At this higher frequency, the large reduction in input resistance from run EB 26 to run EB 29 should manifest itself in a significantly lower noise figure, something very difficult to observe at 8 GHz.

Summarizing, the first successful results for FETs using the mushroom gate structure have been reported. The gate resistance improved dramatically, by about a factor of 6, leaving the source resistance as

the dominant component of the input resistance. Evidence has been given that the source resistance is basically determined by the gate-to-n^+ spacing.

5. COMPARISONS WITH PHOTOLITHOGRAPHIC GATES

In an effort to determine if electron-beam damage is occurring in the gate region during gate exposure, and also to determine FET performance for the MBE material using longer gate lengths and the self-aligned n^+ technology developed for the electron-beam-exposed FETs, two runs were made using the same material as has been used for the electron-beam-exposed FETs, but with the gate exposed using photolithography.

The first run was done using the Varian "NOM" mask set. Its gate length is nominally one micron and the device width is Z = 300 μm. The results are shown in Table V. The device gate lengths were on the order of 1.2 μm. No further analysis was done on the devices to determine what the reason was for the large difference in noise figures for the two devices measured.

TABLE V

NOM Device Results at 8 GHz

Device	NF_m (dB)	G_a (dB)
NOM 1	2.82	8.8
NOM 2	1.87	10.2

The second run was done using the Varian "LNX-100" mask set. This mask set has a nominal gate length of 0.5 micron and a device width, Z, of 240 μm. The results of this run are shown in Table VI. Because of contact difficulties in the photolithography, the gate lengths were 0.9-1.0 micron. It had been hoped to achieve 0.5 micron in order to afford a closer comparison with the electron-beam-exposed devices. Ideally, one would want the same gate lengths as for the electron-beam-exposed devices in order to determine directly whether electron-beam damage is a

problem. These results are to be compared with 1.1 dB at 8 GHz with 0.3 μm gates using electron lithography.

TABLE VI

LNX-100 Device Results

Device	Frequency (GHz)	NF_m (dB)	G_a (dB)
LNX-100-1	8	1.7	9.5
LNX-100-2	10	2.48	10.3
LNX-100-3	10	2.28	8.5

No definitive conclusions were reached concerning the possibility of electron-beam damage in the gate region of the fabricated FETs by comparison with FET runs made on the same material using the same self-aligned process with longer optically-exposed gates. If the noise figures for the optical gates are scaled according to Fukui's noise figure equation[9] from one-micron gate lengths down to a 0.25 value with all of the other parameters the same (which indeed is a good assumption since the material parameters, pinchoff voltage, source resistance, and gate resistance were measured to be virtually the same), a value of 0.65 dB is obtained at 8 GHz. This value is significantly better than the 1.1 dB values actually measured. However, it is believed that Fukui's equation is valid for an aspect ratio of gate length/channel thickness of roughly around 3:1, and hence isn't applicable to the 14:1 ratio of the optically-exposed gates. Hence, the only real way to make a valid comparison is to fabricate devices with long electron-beam-exposed gates.

6. ELECTRON BEAM DAMAGE STUDY

As mentioned in Annual Report No. 3, because of the degradation that occurs in the FET drain characteristic when observed with the 20-keV SEM electron beam, it appears that some material degradation in the channel also occurs when the gate region is exposed with a 20-keV beam.

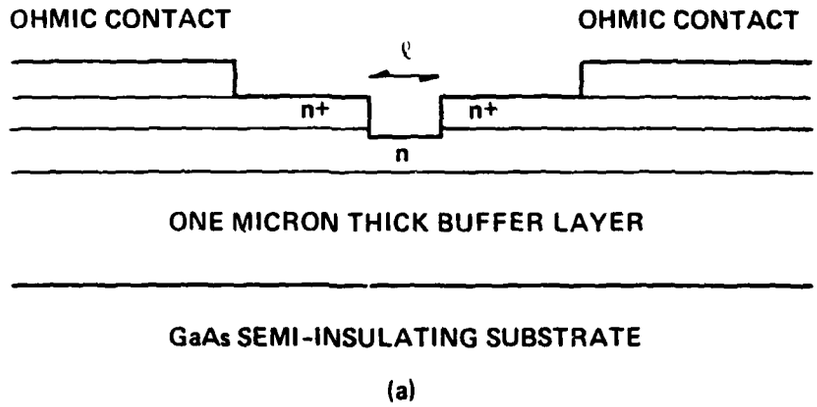
An annealing study done by Pons and Mircea of LEP[10] on electron irradiation-induced defects in GaAs indicates that a 210°C anneal for 150 min significantly reduces the concentration of the defect levels E2-E5 produced by a 1-MeV electron beam. Accordingly, a 2.5-hr anneal at 210-220°C in N_2 was done on several completed devices from run EB 29. The result was that the gate leakage increased (went from 10 μA at 4V to 10 μA at 1V) and the minimum noise figure increased rather than decreased, going from 1.3 to 1.63 dB.

A discussion with A. Zylbersztejn of Thompson-CSF at the U.S.-France Workshop on GaAs Microstructures in Boston, June 8-10, led to the opinion that there is no electron-beam damage in the channel. Zylbersztejn has the effect of deep level traps E1-E5 induced by 1-MeV electron irradiation upon FET properties and gave his opinion that the threshold for damage to GaAs in terms of generation of deep level traps E1-E5 is 200-250 keV (a paper is soon to be published concerning this). He was convinced that the 20-keV level used to expose the gates could do no damage to the channel region.

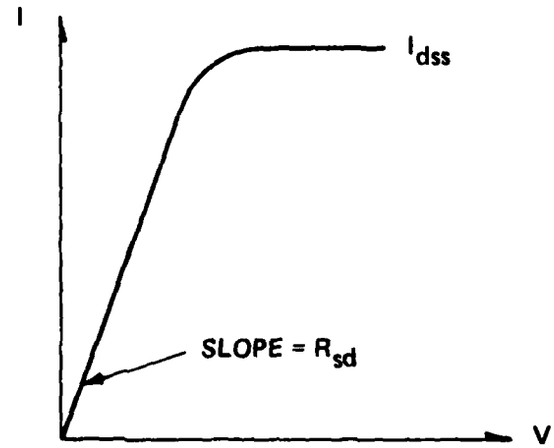
7. VELOCITY OVERSHOOT

A series of experiments was tried to determine additional information about the FET structure presently used, which is not obtainable from the completed FET itself. The regular source-drain ohmic contacts were put down on the same MBE material used for FETs and the n^+ layer was selectively removed (as shown in Fig. 20) using the regular gate process, without the gate deposition. By varying ℓ, the intention was to separate out the contribution of the n^+ layer and the ohmic contact resistance portion of the source resistance, R_s, and also to see if there is any dependence of I_{dss} on ℓ, which would indicate velocity overshoot effects.

Using MBE wafer #490 and the source-drain contact pattern for the single-gate device (Z = 150 microns), the data in Fig. 21 was obtained. The ohmic contact spacing ranged from 2.4-2.6 microns. The material parameters assumed for the interpretation were target values given to the MBE group: 1200 Å of $3.5 \times 10^{17} cm^{-3}$ (Si-doped) covered by 1000 Å of $10^{19} cm^{-3}$ (SnTe-doped). The value of ~2.5 ohms for $\ell = 0$ means that the contribution of the n^+ layer and the ohmic contact resistance to the source resistance would only be 1-1.5 ohms. Figure 21 also shows 1.25 ohms per 1000 Å for the etched region, indicating 2.5 ohms for the total source resistance, since typically the gate-to-n^+ spacing is ~1000 Å for the FETs. This kind of value for R_s was indeed observed for the high-current devices of runs like EB 6, for example. Runs EB 16 and 26, on the other hand, have had values of R_s ranging from 6 to 9 ohms, but then the values of I_{dss} were quite low, ranging from 12 to 17 mA. A gate placed in the etched region would lower the I_{dss} data in Fig. 21, but to what value is not certain, so it is hard to compare the R_{sd} data in Fig. 21 with what actually occurs in a FET. The data does reveal, however, that ohmic contact resistance and the n^+ layer should contribute little to R_s.



(a)



(b)

Fig. 20 Structure (a) and data interpretation (b) used for material evaluation.

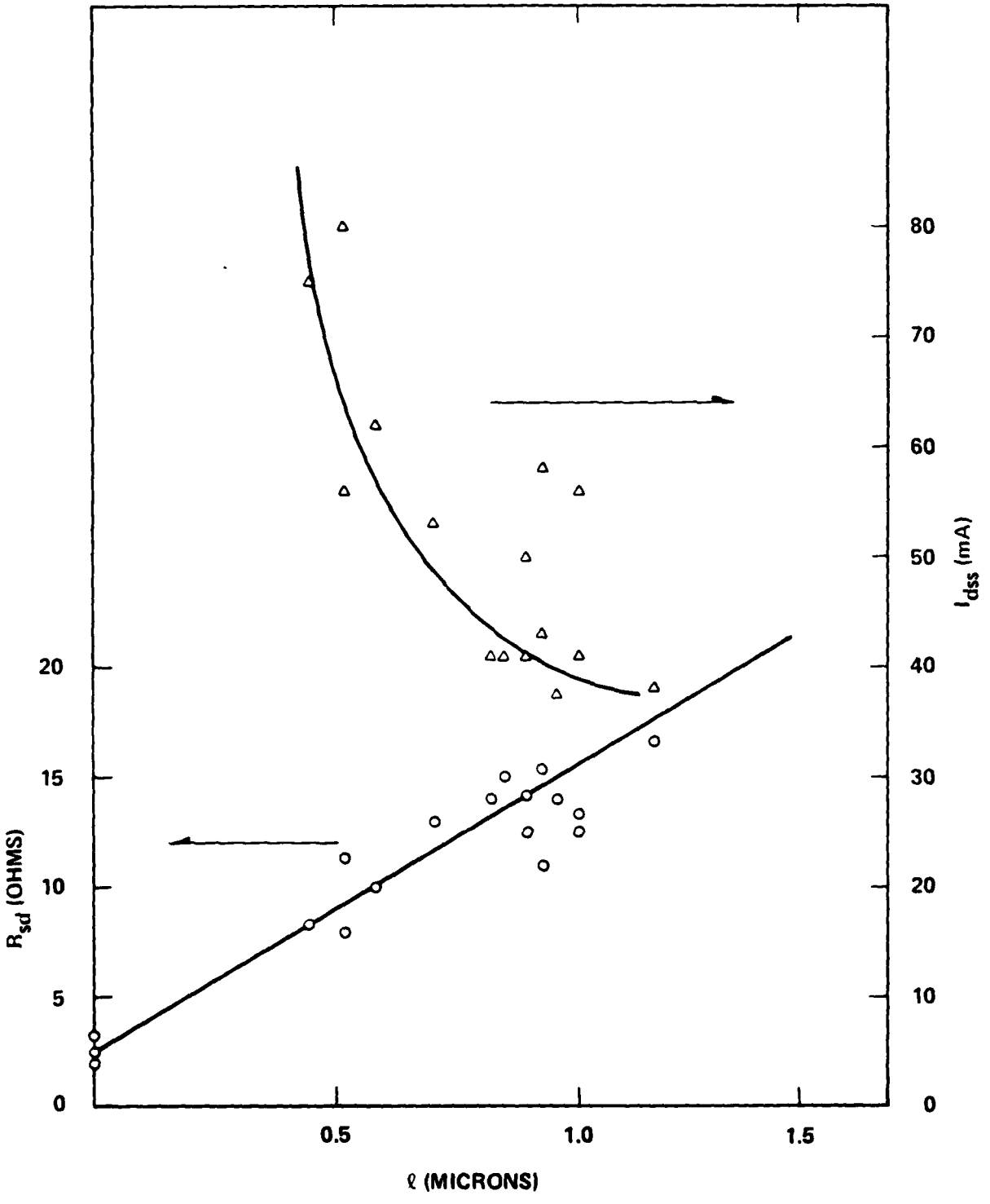


Fig. 21 Data obtained from Fig. 2 structure

The scatter in the data of Fig. 21 is believed to be due to variations in the etched depth (or original epitaxial layer thickness), since the low values of R_{sd} correspond to high values of I_{dss} and vice versa. The marked increase in I_{dss} with decrease in ℓ suggests strong velocity overshoot effects, although carrier enhancement might also explain the variation.

8. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

8.1 Accomplishments and Problems Solved

During this period, the gate resistance was reduced by about a factor of 6 by improving the mushroom gate technology to the point where it could be used in an actual device run. However, the dramatic reduction in gate resistance was accompanied by only a marginal improvement in the measured minimum noise figure of about 0.2-0.3 dB. This is believed due to limitations in the noise-measuring technique, rather than an absence of improvements in device performance.

One of the problems preventing the formation of reliable mushroom-gate structures with the double resist scheme was found to be an increased sensitivity of the scheme to the focus of the electron beam, when compared to using a single layer of resist. This was solved by developing an automatic computer-focusing program to eliminate the subjective judgment of the human operator.

Another problem with the mushroom scheme was found to be the formation of a void in the mushroom structure between its top and its base caused by closure of the resist opening by the deposited metal, the problem that prompted investigation of the mushroom structure in the first place. Further investigation revealed that the evaporating metal forms a virtual source whose size was considerably larger than the actual source size, permitting metal to impinge on the wafer at large angles of incidence. This was solved by using a set of baffles to collimate the evaporation. This resulted in a successful FET run with the mushroom profile gates. This FET run was also made on material with the doping of the n^+ contact layer increased to above $10^{19}cm^{-3}$.

The gate resistance was lowered about a factor of six to around 0.8 ohms, and the source resistance about a factor of two to 3.5 ohms (the device width is 150 microns). Values of 1.1 dB for the noise figure and

13.9 dB for the associated gain were measured at 8 GHz. Better performance than this was expected for such a large reduction in input resistance; problems of matching such a high Q input with the rather lossy microstrip technique may be responsible for an inaccurate measurement of noise figure.

8.2 Recommendations for Future Work

At this point, it appears that with the solution of the first-order fabrication technology problems that the need is for noise measurements at a higher frequency than 8 GHz. The microstrip matching technique used may be sufficiently lossy at 8 GHz to prevent measurement of the true performance capabilities of the device. A test setup for 26 GHz is now nearing completion.

If indeed the true performance has been measured at 8 GHz, then a closer look needs to be taken at the device s-parameters and the noise theory itself to determine the reason why the performance is not a great deal better, given the reduction in input resistance.

Some evidence has been presented to indicate that electron-beam degradation of the channel area is no problem, but the phenomenon of g_m reduction with frequency is still observed and may be worth investigating more fully. Reduction of the source inductance is another area that needs to be addressed for higher frequency operation.

Then, of course, there are the more fundamental and ultimate goals that need to be addressed -- determination of optimum channel thickness and doping for a given gate length and the measurement of velocity overshoot and its dependence upon crystal orientation, as discussed in the Introduction.

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